Abstracts

GaAs MOSFET High-Speed Logic

N. Yokoyama, T. Mimura, H. Kusakawa, K. Suyama and M. Fukuta. "GaAs MOSFET High-Speed Logic." 1980 Transactions on Microwave Theory and Techniques 28.5 (May 1980 [T-MTT] (Special Issue on Gigabit Logic for Microwave Systems)): 483-486.

Enhancement-mode GaAs MOSFET integrated logic shows superior potential for applications in low-power high-speed integrated circuits. The speed / power performance of this logic was investigated by using GaAs MOSFET ring oscillators, fabricated using a low-temperature plasma oxidation technique for gate insulation. With an enhancement-depletion (E/D)-type ring oscillator, a minimum propagation delay of 110 ps per gate is obtained, with a power/speed product of 2.0 pJ. With an enhancement-enhancement (E/E) type, a minimum power/speed product of 26 fJ is obtained, with a 385-ps delay. These performances are equal to or better than those of GaAs MESFET logic, after adjustments are made for gate size. With further refinements in device geometry and improvements in gate oxide, GaAs MOSFET logic will be of great use in high-speed very-large-scale integrated circuits.

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